

Articia S

PRODUCT HIGHLIGHTS

Versatile Chipset for both RISC and X86 Compatible Processors

Support 133MHz Bus Speed

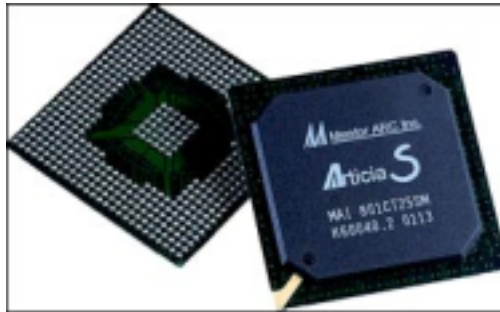
Multi-Function Memory Controller

iMemory

Dual PCI buses (PCI 0 and AGP/PCI 1)

Floating Buffer

Genetic Computing™



Generic Low-Cost Chipset Solution for RISC Processor Based Systems

Articia S is a versatile chipset targeted at 64-bit RISC processor (PowerPC and MIPS) based systems with low power consumption and high system performance.

133MHz Multi-Platform Support

Articia S can support either single or dual CPUs at 133MHz CPU bus speed. In addition to RISC family, Articia S can also support X86 compatible processors.

133 MHz SDRAM Chipset with iMemory Technology

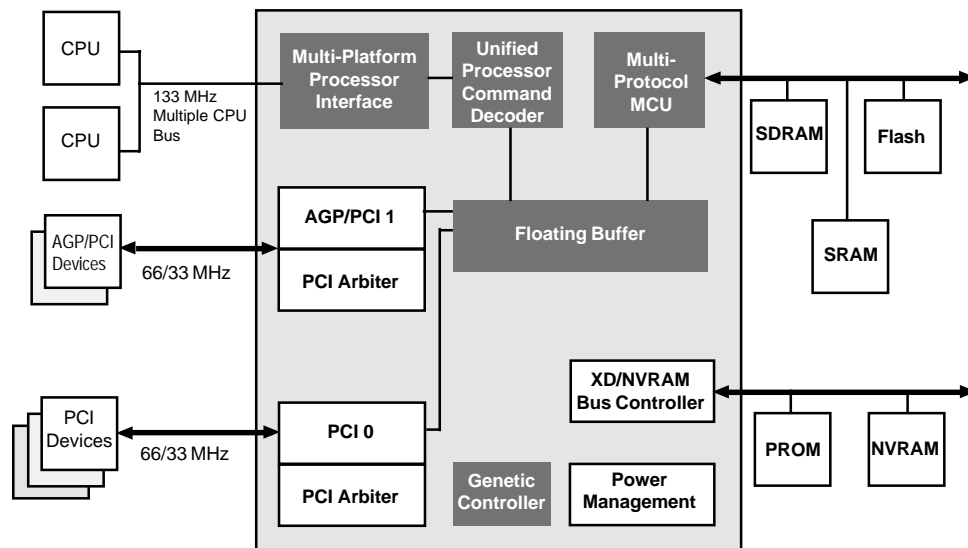
Articia S offers the 72-bit (with ECC) 133MHz memory interface with mixed mode memory support, including SDRAM, Flash/PROM, and SRAM. It also embraces iMemory technology to implement run-time and in-field memory fault recovery functions. As a result, the overall system performance and stability are greatly improved.

First Chipset Provides AGP Support On RISC Processor Based Systems

Articia S supports dual PCI buses: PCI bus 0 and AGP/PCI Bus 1. The AGP/PCI bus 1 can act either as a 66MHz AGP2X bus for enhanced graphics and 3D features or as a second PCI bus at 66/33MHz for optimized PCI performance.

Value-added Features

Articia S also includes the unique Floating Buffer for efficient DRAM bandwidth management and true concurrent performance as well as Genetic Computing™ for system security.



For more information
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Articia S

PRODUCT FEATURES

Processor Support

- PowerPC™ 60X, PowerPC™ 750CX, PowerPC™ 750FX, Motorola's G4, X86 and MIPS R4XXX, R5XXX processors
- SMP support for two processors with three outstanding requests
- Support 133 MHz processor bus speed
- 64-bit CPU address and data parity

Integrated Multiple Function Memory Controller

- 133 MHz memory interface
- 72-bit DRAM Data Path (with ECC) with over 1GB/sec bandwidth
- Support synchronous DRAM up to 8 banks in 4 DIMMs; 8 DRAM pages can be opened simultaneously
- Memory addressable from 8MB to 2GB
- Support 64/128/256/512/1024Mb SDRAM
- Support 2 banks burst mode SRAM on memory bus up to 32 Mbytes
- Support up to 128MB 64-bit PROM space

Floating Buffer

- The smart threading buffer engine for read prefetch/ buffer allocation.
- Zero initial wait state for PCI devices access hits floating buffer, such as 3-1-1-1-...-1 in Read Hit Cycles
- Support page reordering, patented page merge and cache line merge writes according to data transfer requirement
- Prefetch/Read-Ahead and Merge Write features for CPU, PCI 0 and AGP/PCI 1
- Three ports fully concurrent among CPU, PCI 0 and AGP/PCI 1

Fully Synchronous 66/33MHz PCI Bus 0 Interface

- 32-bit, 66/33 MHz PCI interface, 3.3V with 5V tolerance I/O
- Hidden Snoop & Snoop Ahead features with no interference of CPU normal cycles
- Support PCI bus speed 1/1, 1/2, 1/3, 2/3, 1/4 of CPU bus speed
- XD bus decoding and NVRAM support
- PCI bus arbitration unit up to 6 masters
- XD bus PROM/Flash memory addressable up to 8 MB

AGP 2X Bus Interface or 66/33MHz PCI Bus 1 Interface

- 16 piped requests with pipe reordering
- Software transparent one-level TLB translation
- 16-entry GART table cache
- 32-Qword queue for AGP read return queue and 20 QW write data queue
- AGP 2X and sideband address protocol support
- PCI bus arbitration unit up to 2 masters

Power Management Controller (PMC)

- Real time clock alarm and Sleep/Wake-up control logic
- Support processor low power state

iMemory

- Run-Time Memory Fault Recovery

492-pin BGA Package

Order Number: A660BNGP

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